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Measurement of Trap Density in Dielectric Film

The problem:

Dielectric films such as SiO_2 and Si_3N_4 are commonly used in insulated-gate field-effect transistors (IGFET's). The quality of these films has an important bearing on the performance and life expectancy of the transistors. An important determinant of quality in these films is trap density. A trap is a localized imperfection in the film that can accept carriers (electrons and holes) and therefore effect the local charge. A method is needed to determine the trap density and hence to evaluate the film quality.

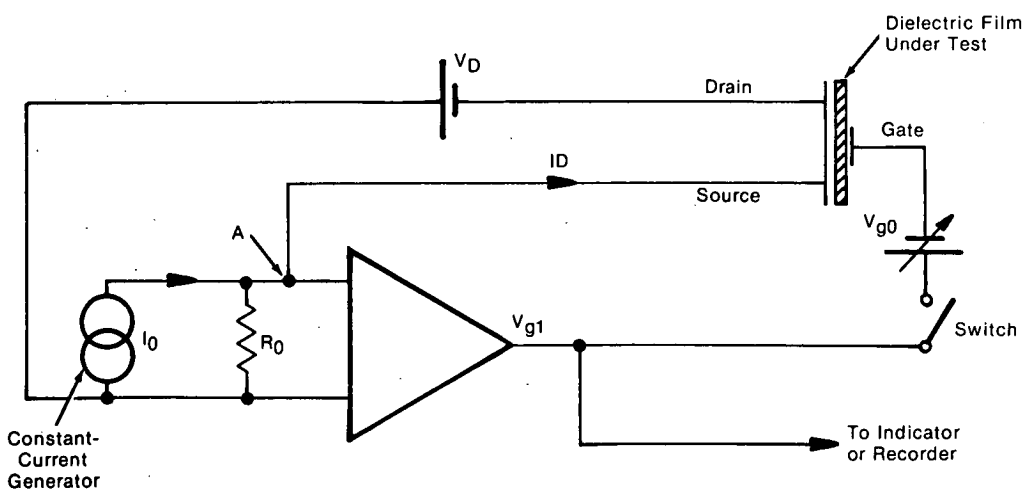
The solution:

A new method has been developed for measuring the trap density of dielectric film using a basic circuit as shown in the illustration.

How it's done:

The test device is connected into the circuit as shown. With a selected constant potential V_{g0} applied to the gate, a constant drain potential V_D drives a drain current I_D through the conducting channel between the source and the drain. A constant-current generator drives a selected reference current I_0 into the junction at A so that the difference in current $I_D - I_0$ passes through resistor R_0. The resulting voltage drop across R_0 is applied to the input of the feedback amplifier.

When I_D equals I_0, the amplifier output is zero. When I_D differs from I_0, the amplifier output voltage V_{g1} is proportional to the change in I_D which corresponds to the change in channel conductance.



Circuit for Determining Trap Density

(continued overleaf)

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When the switch is closed, a selected initial bias potential V_{g0} is applied to the gate. The V_{g0} is selected to give an approximately zero output from the amplifier immediately after closing the switch, i.e., a near-balance condition in which I_D is approximately I_0. This condition is reached by trial and error by repeatedly observing the initial response and adjusting the V_{g0}. The balancing step is necessary to minimize the required amplifier output and thus to reduce feedback error. The algebraic sum of the observed output voltage V_{g1} and the bias V_{g0} at the instant the switch is closed is the unperturbed gate voltage (before space-charge injection). The sum thus determines the field at the interface which is maintained constant during the measurement.

With the switch closed, the output voltage V_{g1} increases, compensating for the injected space charge so that the channel conductance, and thus the interface field, is maintained nearly constant (i.e., $I_D = I_0$). This change in V_{g1} is displayed as a function of time or log time on an oscilloscope or a chart recorder and is used to calculate the trap density.

Note:

Requests for further information may be directed to:

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Reference: TSP75-10204

Patent status:

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning non-exclusive or exclusive license for its commercial development should be addressed to:

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